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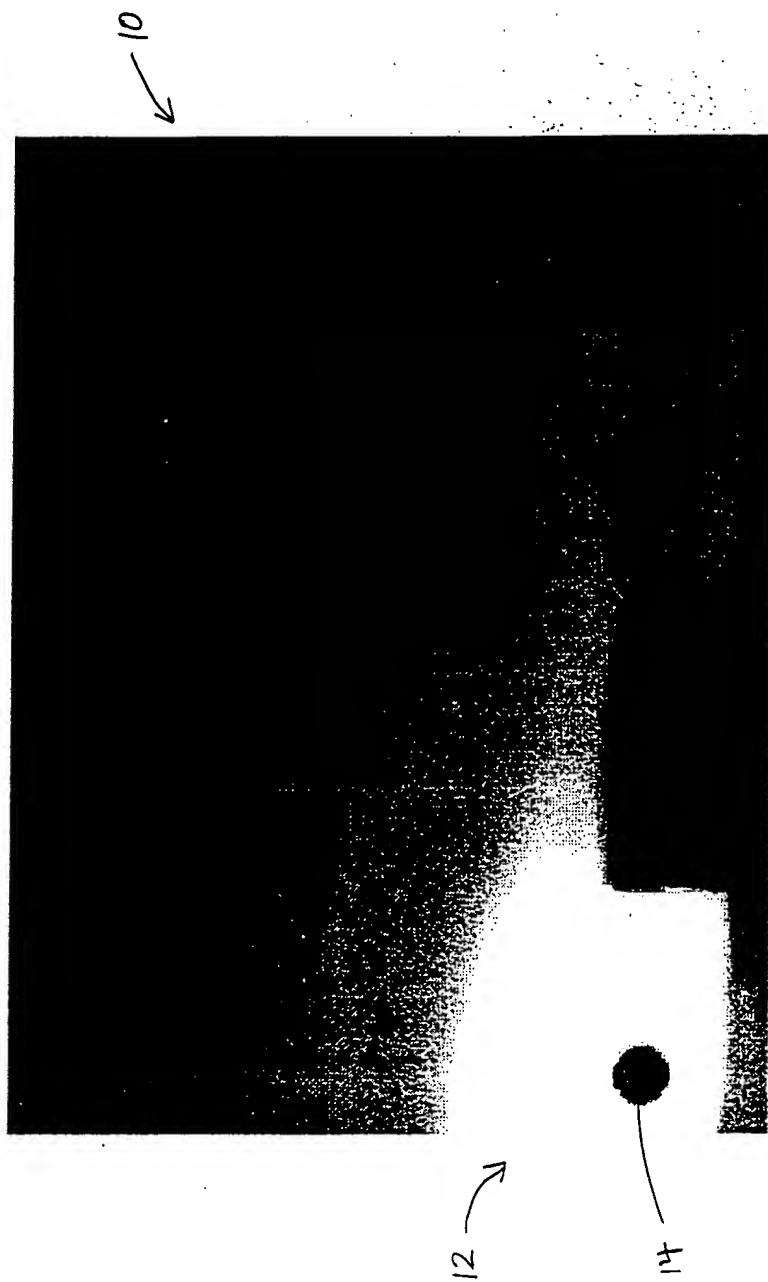


FIG. 1

The diagram illustrates a column signal processor circuit. It begins with a pixel array (20) where each pixel (22) contains a photodiode (26) and a reset transistor (Rst, 30). The photodiode is connected to a vertical signal line (SH_Signal, 44) and a horizontal reset line (RS, 32). The reset transistor (30) is controlled by a reset voltage (V_{rs}) and is connected to the horizontal reset line (RS, 32). The photodiode (26) is connected to the horizontal reset line (RS, 32) and a vertical signal line (SH_Signal, 44). The vertical signal line (SH_Signal, 44) is connected to a series of transistors (46, 52, 58) that form a current source. These transistors are controlled by a common gate voltage (V_{in}, 36) and are connected to a common source (V_{adj}, 60). The output of the current source is connected to a latch (70) and a saturation flag (80). The latch (70) is controlled by a column select signal (82) and a saturation flag (80). The saturation flag (80) is connected to a saturation level (68) and a saturation flag (80). The circuit is labeled with various components and their connections, including a photodiode (26), a reset transistor (Rst, 30), a reset voltage (V_{rs}), a horizontal reset line (RS, 32), a vertical signal line (SH_Signal, 44), a series of transistors (46, 52, 58), a common gate voltage (V_{in}, 36), a common source (V_{adj}, 60), a latch (70), a column select signal (82), and a saturation flag (80).

FIG. 2

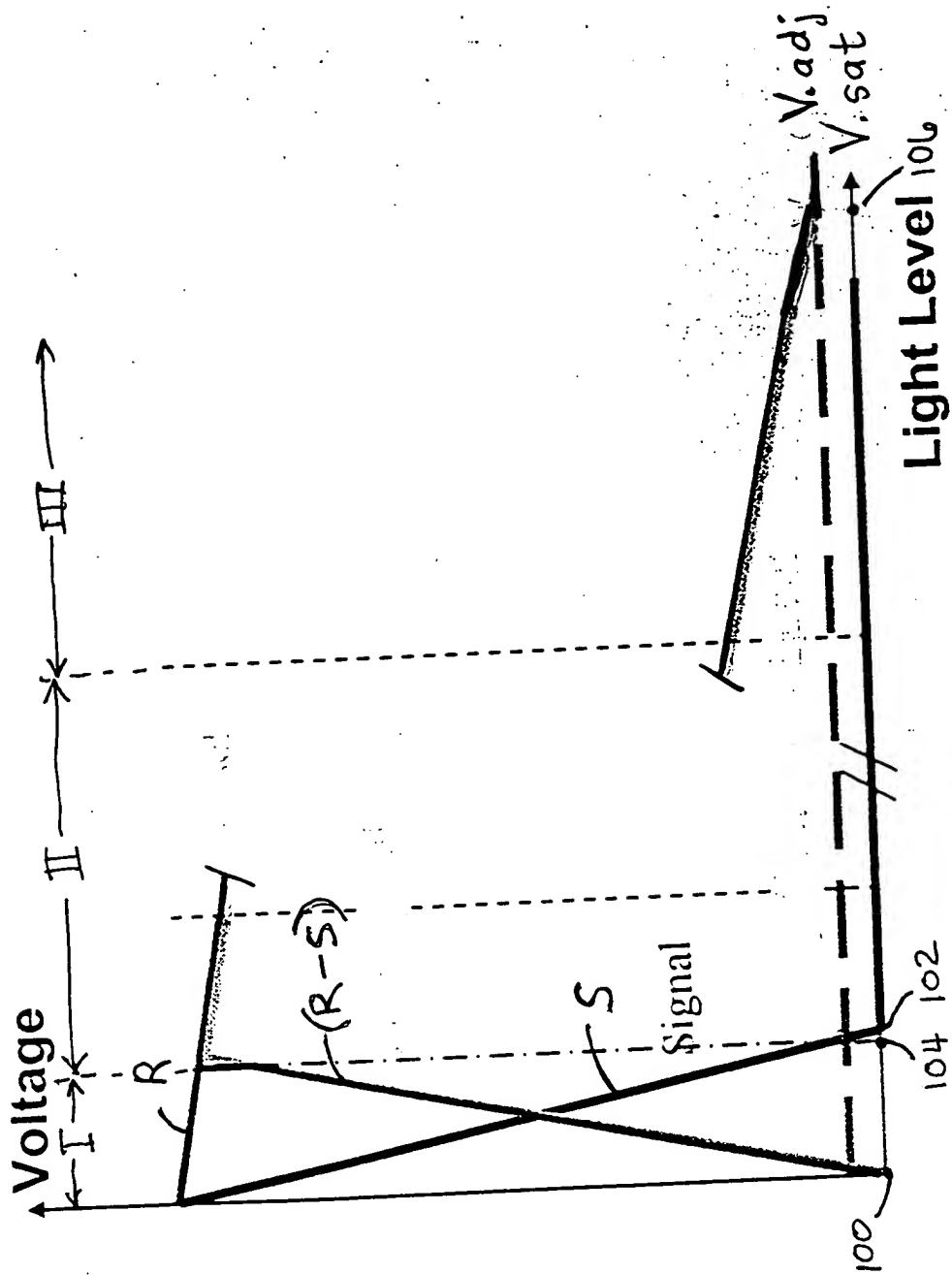


FIG. 3

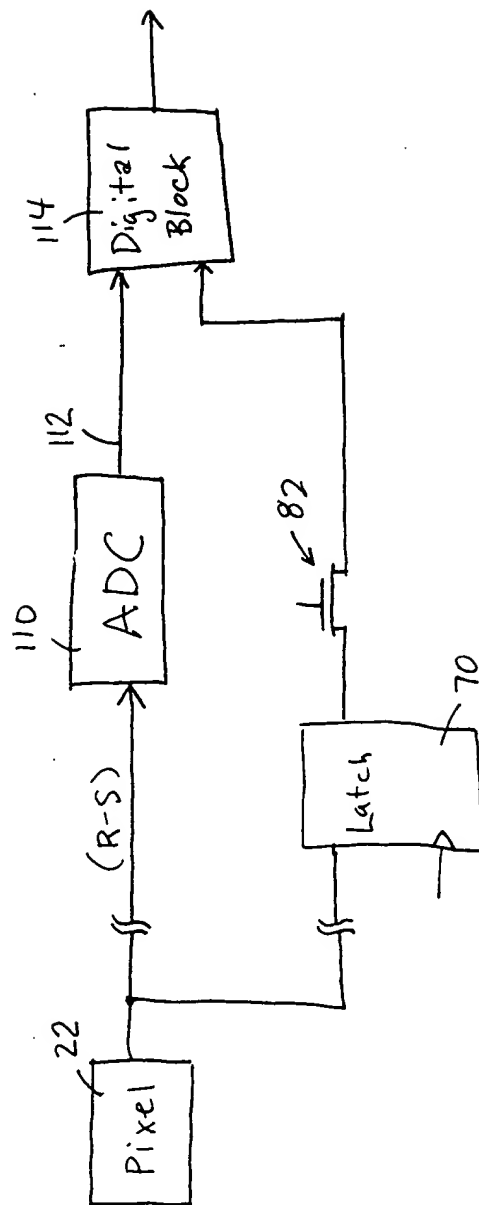


FIG. 4

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